

BIB mitigation with AI

Simons progress report
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Quick Updates

Meetings:

*Meetings are back to the
Wednesday 10a CT slot*

Update from UChicago

- FPGA optimization: turning off DSPs was expected to decrease latency, further study required
- Targeting a more realistic 10–20ns (vs 5 ns) produces sensible results with lower latency + resource usage for Model 1
- SmartPixels for μ C paper draft posted on Slack; **open for comments**

Update from Princeton

- Bit flip studies for LGNs presented at last meeting
- Training with bit flips during training improves robustness to bit flips at inference time, though expected real-world bit flip rate much lower than tested
 - May provide robustness to other distortions of input data, including detector noise